

# ASIC IP Verification Eng

## **Job Description:**

Should have minimum of 5+ yrs of experience in conceptualizing the approach for verification of a design block, construction of test benches and test plans.

Should have experience in using System Verilog , UVM methodologies.

Should possess strong problem solving skills and debug the test failures to root cause the failures.

Mandatory Should have strong ethernet protocol OR PCIE Express layer.

Ability to assimilate verification requirements from complex design specifications and information spread across various standard body specifications, references and manuals.

Job Location : Bangalore

Exp Level : 5 – 12 yrs

Position : ASIC IP Verification Engineer

Mandatory Skills : ASIC, IP Verification, UVM, Verilog, Ethernet protocol, PCIE

Qualification : Any

Please mail your profiles to [contactus@sawitservices.com](mailto:contactus@sawitservices.com)